	L #	Hits	Search Text	DBs	Time Stamp
1	L1	504727	NEC.as.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/06/22 15:29
2	L2	43	1 and (capacitance near adjusting)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/06/22 15:41
3	L3	37	2 and ((@ad<"20020726") or (@rlad<"20020726"))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/06/22 15:30

	L #	Hits	Search Text	DBs	Time Stamp
4	L4	3	3 and "bonding pad"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/06/22 15:40
5	L5	13	("3433937" | "3889133" | "4687949" | "4894791" | "5041741" | "5107153" | "5329174" | "5831457" | "5905398" | "5999042" | "6066973" | "6072351").PN.	US-PGPUB; USPAT; USOCR	2005/06/22 15:31
6	L6	13	("3433937" | "3889133" | "4687949" | "4894791" | "5041741" | "5107153" | "5329174" | "5831457" | "5905398" | "5999042" | "6066973" | "6072351").PN.	US-PGPUB; USPAT; USOCR	2005/06/22 15:33
7	L7	0	("6507232").URPN.	USPAT	2005/06/22 15:33
8	L8	526	Elpida.as.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/06/22 15:34

	L #	Hits	Search Text	DBs	Time Stamp
9	L9	3	8 and (capacitance near adjusting)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/06/22 15:35
10	L10	13981	Miyazawa.in.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/06/22 15:35
11	L11	6	10 and (capacitance near adjusting)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/06/22 15:36

	L #	Hits	Search Text	DBs	Time Stamp
12	L12	27005	Izumi.in.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/06/22 15:36
13	L13	1	12 and (capacitance near adjusting)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/06/22 15:36
14	L14	38714	Matsui.in.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/06/22 15:40

	L #	Hits	Search Text	DBs	Time Stamp
15	L15	6	14 and (capacitance near adjusting)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/06/22 15:41

US-PAT-NO: 6507232

DOCUMENT-IDENTIFIER: US 6507232 B2

TITLE: Semiconductor device which can be set to predetermined capacitance value without increase of delay time

---------- KWIC ---------

Application Filing Date - AD (1):
19990624

Assignee Name - ASNM (1):
NEC Corporation

Brief Summary Text - BSTX (3):
The present invention relates to a semiconductor device. More particularly, the present invention relates to a semiconductor device having an element for **adjusting a capacitance** value of an input terminal.

Brief Summary Text - BSTX (6):
Traditionally, the technique as shown in FIG. 1 as an element (hereafter, referred to as a **capacitance adjusting** element) to adjust such a capacitance value of an input terminal is disclosed in Japanese Laid Open Patent Application (JP-A-Heisei 3-138962).

Brief Summary Text - BSTX (7):
As shown in FIG. 1, an input circuit section 502 is connected through a wiring 508 to a **bonding pad** 500. A plurality of MOS-type capacitance elements 504, 505 and 506 are located adjacently to the **bonding pad** 500. A lower electrode of these MOS-type capacitance elements 504, 505 and 506 is a grounded silicon substrate. Respective upper electrodes are provided on the silicon substrate through dielectric film formed of silicon oxide. The respective upper electrodes are connected through fuses (not shown) to the **bonding pad** 500.

Brief Summary Text - BSTX (8):

Since the fuses of the MOS-type capacitance elements 504, 505 are not cut off, the capacitance (capacities) thereof are connected to the **bonding pad** 500. Since the fuse of the MOS-type capacitance element 506 is cut off, the capacitance of the MOS-type capacitance element 506 is not connected to the **bonding pad** 500. In this way, the utilization of the fuse enables the connected capacitance value to be adjusted.

Brief Summary Text - BSTX (10):

The inventor of the present invention noticed that an input circuit of the input circuit section was composed of insulated gate field effect transistors (hereafter, referred to as MOS-transistors). As a result, the inventor of the present invention thought that the MOS-transistors as **capacitance adjusting** elements (MOS-transistors instead of the MOS-type capacitance elements 504, 505 and 506) should be formed, separately from the MOS-transistors for operating the input circuit section (the MOS-transistor of the above-mentioned input circuit).

Brief Summary Text - BSTX (11):

The MOS-transistors as **capacitance adjusting** elements is formed with the present device process of the MOS-transistor. Thereby a gate oxide film serving as a capacitance insulating film of the **capacitance adjusting** element can be thinned to about 10 nm to thereby reduce an area occupied by the **capacitance adjusting** element. Moreover, it can be formed simultaneously with the MOS-transistor for operating the input circuit section. Thus, the process of forming the **capacitance adjusting** element is not additionally required.

Brief Summary Text - BSTX (12):

For example, if using the device process to form the **capacitance adjusting**

element composed of the MOS-transistors each having a gate oxide film of about
10 nm, the area thereof can be reduced to 1/6 or less of an area of a PN
junction type capacitance element having the same performance.

Brief Summary Text - BSTX (13):
In this case, it is necessary that an input protecting resistor is provided
between the **bonding pad** and each of the MOS-transistor for operating the input
circuit section and the MOS-transistor as the **capacitance adjusting** element, to
protect the electrostatic breakdown in each gate oxide film.

Brief Summary Text - BSTX (14):
Here, a delay amount when an input signal entered to the **bonding pad** is
transmitted to the input circuit section is determined by a product of a
resistor value R and a capacitance value C between the **bonding pad** and the
input circuit section.

Brief Summary Text - BSTX (15):
A value of a parasitic resistance of the wiring is sufficiently smaller than
the resistor value of the input protecting resistor. Thus, the resistor value
R is determined in accordance with a resistor value R.sub.P of the input
protecting resistor. On the other hand, the capacitance value C includes a
parasitic capacitance C.sub.A of element and wiring which is parasitic at a
node (contact) between the input circuit section and the input protecting
resistor and a capacitance value C.sub.B of the MOS-transistor serving as the
capacitance adjusting element. Hence, the input signal entered to the **bonding**
pad is delayed by a time corresponding to a time constant
R.sub.P.times.(C.sub.A +C.sub.B) when the input signal is transmitted to the
input circuit section.

Brief Summary Text - BSTX (16):
FIG. 2 shows a signal wave form at this time. In FIG. 2, a symbol 610
denotes a signal wave form in the **bonding pad**. A symbol 620 denotes

a signal
wave form in the input circuit section transmitted under the delay of the time
corresponding to the time constant R.sub.P.times.(C.sub.A +C.sub.B).

Brief Summary Text - BSTX (19):
Thus, the layout is typically designed such that the **bonding pad** and the
input circuit section are as close as possible to each other, so as to suppress
the parasitic capacitance C.sub.A of the device and the wiring which is
parasitic at the node between the input circuit section and the input protecting resistor. In a case of 64 MSDRAM, the parasitic capacitance C.sub.A
is about 0.1 pF.

Brief Summary Text - BSTX (20):
On the other hand, parasitic capacitance values at a pad, an input protecting element, a lead frame and the like between the **bonding pad** and the
input circuit of the device other than the above-mentioned parasitic capacitance C.sub.A are about 1.7 pF. Thus, in order to satisfy the standard
value, it is necessary to further add (connect) a capacitance C.sub.B of about
1.5 pF to thereby set the capacitance of the input terminal to the intermediate
value 3.3 pF in total. The value R.sub.P of the input protecting resistor is
about 350 .OMEGA.. Hence, the delay time of the signal in the device is
represented in time constant as follows:

Brief Summary Text - BSTX (22):
These delay amounts are generated as the relative delay time of the device
operation with respect to the signal entered in the device. Thus, they are
regarded as the deterioration of the performance of the device. As mentioned
above, the conventional technique shown in FIG. 1 needs the large area in order
to form the **capacitance adjusting** element. Thus, the integration degree is
sacrificed. Also, it additionally needs the process of forming the **capacitance
adjusting** element. Hence, the manufacturing process becomes complex, which
results in interference with reduction of a manufacturing cost.

Brief Summary Text - BSTX (23):
On the other hand, if trying to utilize the device process of the MOS transistor directly when forming the **capacitance adjusting** element, this trial causes the delay of the input signal to be larger so that the device performance is deteriorated.

Brief Summary Text - BSTX (24):
Therefore, an object of the present invention is to provide a semiconductor device which can adjust an input terminal (**bonding pad**) to have a predetermined capacitance value without needing a large area and increasing a manufacturing process and further making a delay time of an input signal larger.

Brief Summary Text - BSTX (31):
The present invention has been made to solve the above-described problems of the conventional semiconductor device. An object of the present invention is to provide a semiconductor device which can adjust an input terminal (**bonding pad**) to have a predetermined capacitance value without needing a large area and increasing a manufacturing process and further making a delay time of an input signal larger.

Brief Summary Text - BSTX (44):
Also in this case, the input and output section is a **bonding pad**.

Brief Summary Text - BSTX (46):
In order to achieve yet still another aspect of the present invention, a semiconductor device includes an input and output section to and from which a signal is inputted or outputted, an internal circuit section for receiving the signal inputted to the input and output section or for outputting the signal via the input and output section, a first wiring for connecting the input and output section to the internal circuit section and a **capacitance adjusting** section for **adjusting a capacitance** connected to the input and output section, wherein the **capacitance adjusting** section is connected to a second

wiring which
is different from the first wiring and is connected to the input and output
section without being connected to the internal circuit section.

Brief Summary Text - BSTX (48):
Also in this case, the semiconductor device further includes a second
protecting resistor connected between the input and output section and the
capacitance adjusting section on the second wiring to protect the **capacitance**
adjusting section.

Detailed Description Text - DETX (5):
This input circuit section 102 is connected through a first input protecting
resistor 101 to a **bonding pad** 100 with a wiring 108. The first input
protecting resistor 101 is made of polysilicon and has a resistance of 350
.OMEGA.. If a serge voltage is entered in the **bonding pad** 100, the first input
protecting resistor 101 protects the gate insulating film Ek of the
MOS-transistor 110 such that the electrical breakdown in the gate insulating
film Ek is not occurred.

Detailed Description Text - DETX (6):
In a **capacitance adjusting** element section 103, many MOS-transistors are
arrayed in a direction (a lateral direction in FIG. 3) as the **capacitance**
adjusting element. In FIG. 3, three MOS-transistors 104, 105 and 106 are
illustrated as a example. Each of the MOS-transistors 104, 105 and 106 serving
as the **capacitance adjusting** elements is composed of a gate electrode G formed
on a gate insulating film E, an N-type source region S and an N-type drain
region D.

Detailed Description Text - DETX (10):
Of the MOS-transistors 104, 105 and 106, the gate electrodes G of the
MOS-transistors 104, 105 are connected through a first portion 109A of a wiring
109 to one end of a second input protecting resistor 107. The wiring 109 is
formed with a metallic film of chromium, aluminum and the like. The

other end
of the second input protecting resistor 107 is connected through the wiring 109
to the **bonding pad** 100. The second input protecting resistor 107 is formed of
polysilicon and has a resistance of 350 .OMEGA..

Detailed Description Text - DETX (11):
Accordingly, the MOS-capacitance values of the MOS-transistors 104, 105 are
entered (added or connected) to the **bonding pad** 100. Then, if the serge
voltage is induced in the **bonding pad** 100, the second input protecting resistor
107 prevents the gate insulating films E of the MOS-transistors 104, 105 from
being statically broken down. The second input protecting resistor 107 stops
an occurrence of an electrical breakdown in the gate insulating films E of the
MOS-transistors 104, 105.

Detailed Description Text - DETX (12):
On the other hand, the gate electrode G of the MOS-transistor 106 is
connected through a second portion 109B of the wiring 109 to the ground. Thus,
the MOS-capacitance value of this MOS-transistor 106 is not entered (added or
connected) to the **bonding pad** 100.

Detailed Description Text - DETX (14):
The pattern of the wiring 109 determines which gate electrode G of the
MOS-transistors 104, 105 and 106 of them 104, 105 and 106 is connected through
the first portion 109A of the wiring 109 and the second input protecting
resistor 107 to the **bonding pad** 100 and which gate electrode G of the
MOS-transistors 104, 105 and 106 is connected through the second portion 109B
of the wiring 109 to the ground. Thus, the pattern of the wiring 109 is
designed such that the **bonding pad** 100 obtains a predetermined capacitance
amount.

Detailed Description Text - DETX (16):
The MOS-transistors 104, 105 and 106 have the same MOS-capacitance value

C104=C105=C106. Thus, as shown in FIG. 3, the MOS-transistors whose gate electrodes G are connected to the **bonding pad** 100 (104 and 105 in FIG. 3) are selected from one side (a left side of FIG. 3) in the array direction of the MOS-transistors 104, 105 and 106, and the MOS-transistor (106 in FIG. 3) whose gate electrode G is connected to the ground is selected from the other side (a right side of FIG. 3). This manner makes the pattern configuration of the wiring 109 (109A, 109B) easier.

Detailed Description Text - DETX (17):

In this embodiment, the MOS-transistors 104, 105 and 106 serving as the **capacitance adjusting** element are formed under the same configuration as the MOS-transistor 110 serving as the circuit element. Thus, the area required to attain a desirable capacitance can be reduced to further simplify the manufacturing process.

Detailed Description Text - DETX (18):

Moreover, the second input protecting resistor 107 for protecting the static breakdown in the MOS-transistors 104, 105 and 106 of the **capacitance adjusting** element section 103 is provided separately from the first input protecting resistor 101 for protecting the static breakdown in the MOS-transistor 110 for operating the input circuit section 102. Hence, the input signal inputted to the **bonding pad** 100 can be transmitted to the input circuit section 102 under a short delay time, regardless of the presence of the **capacitance adjusting** element section 103.

Detailed Description Text - DETX (19):

As mentioned above, the time constant if this embodiment is not used, is represented by R.sub.P.times.(C.sub.A +C.sub.B) when letting the parasitic capacitance of the element and the wiring which is parasitic at the node between the input circuit section and the input protecting resistor be C.sub.A,

the capacitance of the **capacitance adjusting** element be C.sub.B, and the resistance of the input protecting resistor be R.sub.P. So, we have a large value of 350 .OMEGA..times.(0.1 pF+1.5 pF)=560 pS.

Detailed Description Text - DETX (20):
However, in the configuration of this embodiment, the capacitance C.sub.B of the **capacitance adjusting** element has no influence on the delay in the transmission of the signal. Thus, the time constant is represented by R.sub.P.times.C.sub.A. So, the delay time of the signal in the device after the input protecting resistor is 350.OMEGA..times.0.1 pF=35 pS in time constant. Hence, this is a sufficiently small delay amount. That is, this shortens the delay time from an external signal 610, as shown in a wave form 630 of FIG. 2.

Detailed Description Text - DETX (22):
In the second embodiment shown in FIG. 4, MOS-capacitance values of MOS-transistors 204, 205 and 206 for the **capacitance adjusting** element are increased in sequence. That is, let the MOS-capacitance value of the transistor 204 be C204, the MOS-capacitance value of the transistor 205 be C205, and the MOS-capacitance value of the transistor 206 be C206. So, we have the relation of C204<C205<C206.

Detailed Description Text - DETX (25):
Since the MOS-capacitance values different from each other are prepared in this second embodiment, this is suitable for the precise control of the value of the capacitance connected to the **bonding pad** 100. In the first and second embodiments, each of the **capacitance adjusting** elements 104, 105, 106, 204, 205 and 206 has the source region S and the drain region D. Thus, they can be manufactured similarly to the MOS-transistor serving as the circuit element.

Detailed Description Text - DETX (26):

On the contrary, if the existences of the drain region D and the source region S are not desirable as the MOS-capacitance, the **capacitance adjusting** element section 103 is masked when forming the source region Sk and the drain region Dk of the MOS-transistor 110 serving as the circuit element. Accordingly, the formations of the source region S and the drain region D can be omitted as in the third embodiment of FIG. 5 and the fourth embodiment of FIG. 6.

Detailed Description Text - DETX (31):

According to the above-mentioned first to fourth embodiments, the MOS-transistors 104 to 206 in which the MOS-device process is followed in order to make the occupation areas smaller and then the thin gate insulating films E are used as the dielectric films, or the MOS-type capacitance elements 304 to 406 in which the source and drain regions are omitted and similarly the thin dielectric films E are used are used as the **capacitance adjusting** element. Thus, even if the input protecting resistor 107 is required in order to protect the static breakdown in the thin gate insulating film E, this input protecting resistor 107 is the component different from the input protecting resistor 101 for protecting the static breakdown provided between the **bonding pad** 100 and the input circuit section 102. Hence, the above-mentioned embodiments can avoid the undesirable delay of the input signal.

Detailed Description Text - DETX (32):

As mentioned above, according to the present invention, the MOS-transistors in which the MOS-device process is followed to make the occupation areas smaller and then the thin gate insulating films are used as the dielectric films, or the MOS-type capacitance elements in which the source and drain regions are omitted and similarly the thin dielectric films are used are used as the **capacitance adjusting** element. Thus, even if the input protecting

resistor is required in order to protect the static breakdown of the thin gate insulating film, this input protecting resistor is the component different from the input protecting resistor for protecting the static breakdown provided between the **bonding pad** and the input circuit section. Hence, the present invention can avoid the undesirable delay of the input signal.

Claims Text - CLTX (7):
7. A semiconductor device according to claim 1, wherein said input and output section is a **bonding pad**.

Claims Text - CLTX (12):
12. A semiconductor device comprising: an input and output section to and from which a signal is inputted or outputted; an internal circuit section for receiving said signal inputted to said input and output section; a first wiring for connecting said input and output section to said internal circuit section; a **capacitance adjusting** section for **adjusting a capacitance** connected to said input and output section, wherein said **capacitance adjusting** section is connected to a second wiring which is different from said first wiring and is connected to said input and output section without being connected to said internal circuit section; a first protecting resistor connected between said input and output section and said internal circuit section on said first wiring to protect said internal circuit section; and a second protecting resistor, provided on said second wiring that is different from said first wiring, said second protecting resistor being connected between said input and output section and said **capacitance adjusting** section to enable a signal received at said input and output section to be transmitted to the internal circuit section under a reduced time delay.